Monolithic Integration Design of GaN-based Power Chip Including Gate Driver for High-Temperature DC-DC Converters

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Power integration is essential for the fully utilization of advanced GaN devices in power conversion applications due to the reduced parasitic inductance, low on-state resistance, and high-temperature operation. This paper presents a GaN-based monolithic integration design with optimized gate drivers for high-temperature DC-DC converters. Four different gate drivers are experimentally evaluated for integration with boost converters based on enhancement (E)-mode AlGaN/GaN Metal-Insulator-Semiconductor Heterojunction-Field-Effect-Transistors (MIS-HFETs). The optimized gate driver, consisting of DCFL (Direct-Coupled FET Logic) inverters and a buffer amplifier, can operate over a wide temperature range (from 25 °C to 250 °C). Furthermore, a 100 kHz, 5 V/11 V (V_{IN}/V_{OUT}) boost converter prototype with the proposed monolithic integration design was built and found to operate successfully under high temperatures up to 250 °C. These results validate the advantages of GaN-based monolithic integration techniques in achieving high temperature, high power density, and high efficiency power converters.

1. Introduction

AlGaN/GaN heterojuntion based power transistors have excellent performance in high frequency and high temperature operation regimes owing to their superior properties. High temperature power converters are gaining more and more attention in applications under extreme environment, such as oil drilling, aviation and hybrid electric vehicles.[1-4] These high temperature converters require high temperature (HT) gate drivers. The wide band gap devices, such as SiC or GaN, are promising candidates for HT gate drivers for harsh environmental applications.[5] Commercial gate drivers are normally based on Si Complementary Metal Oxide Semiconductor (CMOS) technology, but these gate drivers cannot operate beyond 125 °C due to the limitation of Si material.[3] Gate driver integrated circuits (ICs) using silicon-on-insulator (SOI) technology can enable SiC converters to operate at temperature > 200 °C.[4] GaN-based ICs have shown excellent performance at 250 °C[6-8] or even higher than 300 °C.[9-11] For GaN-based power devices, Si and SiC based drivers do not match GaN fabrication from process integration point of view. Hence, a monolithic integration of GaN-based driver with power switching device on a chip is highly recommended, due to reduced chip area, parasitic inductances and capacitances.[12, 13]

Recent studies have been reported to monolithically integrate drivers with power transistors for DC-DC converters as summarized in Table I. [4, 14-17]. Although most of these studies exhibit superior performance of GaN ICs at room temperature, seldom reports show converters with integrated GaN drivers for HT applications. In this work, we monolithically integrated GaN based gate drivers with an E-mode GaN power transistor for HT DC-DC boost converters, to fully exploit the high temperature performance offered by GaN devices. The E-mode AlGaN/GaN MIS-HFETs used in this work can enable strong immunity to large gate overshoots in GaN-based ICs, due to large gate swings.[18] The integrated GaN driver is consisted of Direct Coupled FET Logic (DCFL) inverters[8-11, 15, 19] and a buffer stage.[15, 17, 20] A detailed study of high temperature AC performance of integrated GaN drivers and boost converters is presented, and the impact of inverter size and buffer stage width on driving capability are systematically studied. The GaN-based boost converter (V_{IN}/V_{OUT} = 5 V/11 V at 100 kHz) with the optimized gate driver showed good performance even at high temperatures up to 250 °C.

Table I. Comparison of DC-DC Converters with HT Gate Drivers

Design	**[4]**	**[14]**	**[15]**	**[16]**	**[17]**	**This Work**
Year	2015	2009	2014	2016	2017	2019
Technology	SiC	1.5 µm E-mode GaN-HEMT	0.5 µm E-mode P-AlGaN HEMT	0.15 µm D-mode GaN-HEMT	3 µm E-mode GaN MIS-HFET	3 µm E-mode GaN MIS-HFET
Gate Driver	SOI driver	Not included	GaN driver	GaN driver	GaN driver	GaN driver
Passive	Discrete	Integrated (diode)	Integrated (driver)	Integrated (driver)	Simulated	Integrated (driver)
Converter	Buck	Boost	Buck	Buck	Buck	Boost
V_{IN}/V_{OUT}	600V/N.A	10V/21V	12V/1.8V	20V/14V	100V/50V	5V/11V
$V_{g,max}$	NR	< 5 V	< 8 V	NR	15 V	12 V
Temperature	200 °C	RT	RT	RT	200 °C	250 °C
Area	Board	w/o driver	11.7 mm^2	5.52 mm^2	Simulated	2.9 mm^2

2. Experimental methods

The AlGaN/GaN epitaxy used in this work consists of a 4.2 µm GaN buffer on a Si substrate, a 21 nm $Al_{0.25}Ga_{0.75}N$ barrier and 1 nm GaN cap layer. The fabrication process started with mesa etching, and the Au-free source and drain ohmic contacts were formed by Ti/Al/Ni/TiN (25/125/45/55 nm) evaporation followed by a rapid thermal anneal (RTA) at 800 °C.

Both depletion (D)-mode MIS-High Electron Mobility Transistors (HEMTs) and E-mode MIS-HFETs were fabricated on the same substrate, with the structure shown in Fig. 1 (a). 150 nm plasma enhanced chemical vapor deposition (PECVD) SiN_x was deposited as passivation layer and an etching hard mask for the E-mode gate recess; the E-mode devices were formed by digital etching.[21, 22] The digital etching was performed by using O_2 plasma treatment at the GaN surface for 3 minutes at 60 °C with an RF (radio frequency) power of 100 W. Afterwards, the oxidation layer was removed by wet etching in 1:10 hydrochloric acid for 1 minute. After 40 cycles of digital etching, the full recess depth of around 22 nm was verified by atomic force microscopy (AFM) with a slow etch rate of about 0.55 nm per

cycle, shown in Fig. 1 (b) and Fig. 1 (c). A 20 nm atomic layer deposition (ALD) Al_2O_3 gate dielectric layer for E/D-mode devices was deposited followed by the evaporation of Ni/TiN as the gate metal.

Fig. 2 shows the DC characteristics of discrete E-mode MIS-HFETs and D-mode MIS-HEMTs on the same chip with gate GaN drivers and power transistors. At 25 °C, the threshold voltage (V_{th}) is +1.5 V and the maximum output current ($I_{DS,\ max}$) is 150 mA/mm (V_{DS}= 10 V) for E-mode devices, while V_{th} is -8.5 V and $I_{DS,\ max}$ is 265 mA/mm (V_{DS}= 10 V) for D-mode devices. When temperature is increased up to 250 °C, both D-mode and E-mode devices show degraded performance. At 250 °C, the V_{th} is +1.1 V and the $I_{DS,\ max}$ decreases to 72 mA/mm for E-mode devices, while D-mode MIS-HEMTs show a V_{th} of -8.8 V and a decreased $I_{DS,\ max}$ of 150 mA/mm. The decrease of output current is due to degradation of channel mobility.[23, 24] Additionally, both E-mode and D-mode devices show an increased drain leakage current about 1.6 mA/mm and 9.2 mA/mm at 250 °C, respectively. The increased leakage current at high temperatures has also been observed in ref.[10, 11].

For integrated drivers, an additional PECVD SiN_x passivation layer and a metal of Al were deposited to connect separate devices in GaN ICs platform. Table II shows four types of drivers fabricated on the same chip; they share the same gate length of L_G=3 μm, gate to source distance L_{GS}=5 μm and gate to drain distance L_{GD}=10 μm, but have different numbers and width of DCFL inverters, and different buffer width as well. The circuit diagram and a photograph of driver No. 3 are shown in Fig. 3.

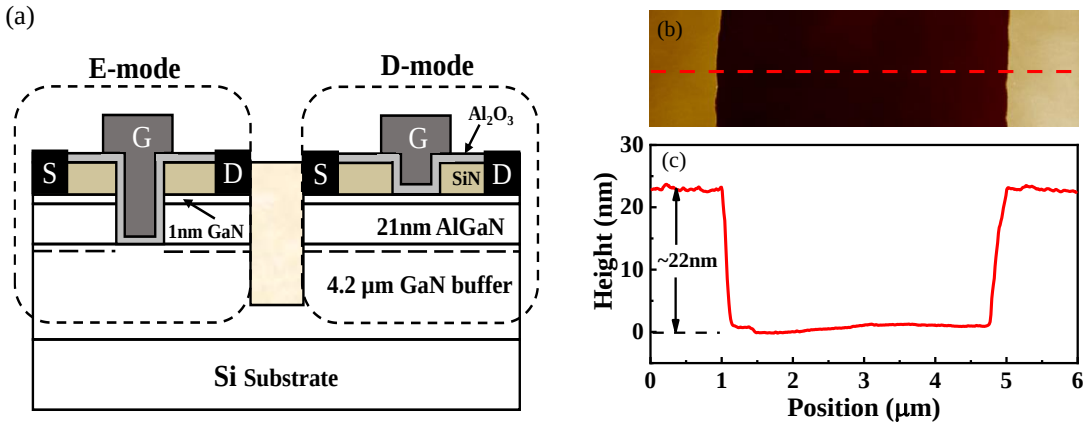

Fig.1 (a) Schematic diagram of E-mode MIS-HFETs and D-mode MIS-HEMTs. (b) Top view and (c) cross section profile (cut from red dash line) of gate trench in E-mode device.

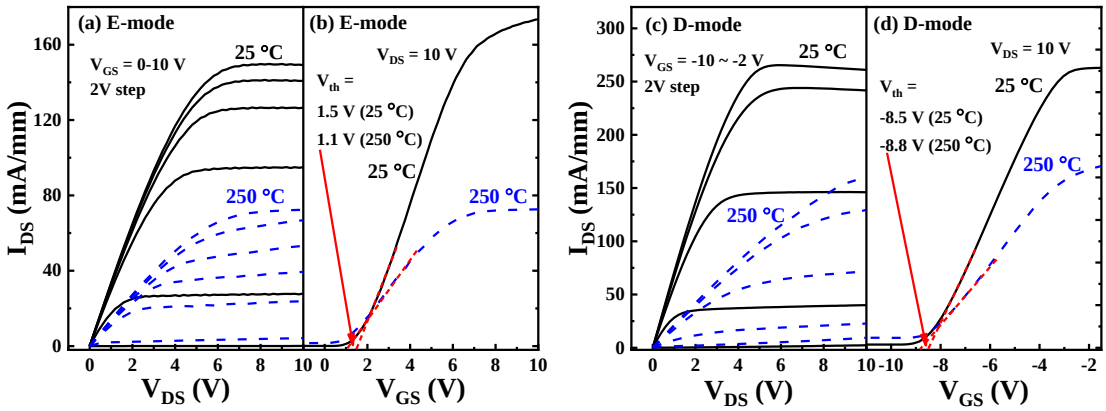

Fig. 2 Output and transfer characteristics of E-mode MIS-HFETs (a) and (b), D-mode MIS-HEMTs (c) and (d) at 25 °C and 250 °C. (Device dimension: L_{GS} /W_G /L_G /L_{GD} =5/50/3/10 μm).

Table II. A list of four types of integrated drivers

Design	**No. 1**	**No. 2**	**No. 3**	**No. 4**
D/E mode width (DCFL inverter)	10/200 μm	50/2000 μm	10/200 μm	50/2000 μm
Number of inverters	2	2	3	3
Buffer width (E_{B1} and E_{B2})	No	No	500 μm	2000 μm

3. Results and discussion

3.1 Gate Driver Test

The circuit diagram of driver measurement is shown in Fig. 3, and the dynamic output waveforms V_{GS} for 4 different drivers are shown in Fig. 4 (a). V_{GS} refers to the voltage between output voltage of each gate driver and ground, which is equal to the voltage applied on the power switching device. At room temperature with a frequency of 100 kHz, all drivers have similar rise and fall time (< 0.5 μs), except No. 1 which has a larger rise time around 2 μs but a relatively low fall time (< 0.5 μs). The large rise time of driver No. 1 is due to the small width of 10 μm of D-mode devices, and has no relationship with the width of E-mode devices as shown in Fig. 4 (b). The rise time of single-stage inverters, which have the same D-mode width (10 μm) as No. 1, is almost unchanged for different D-mode widths of inverters, ranged from 100 μm to 500 μm. Additionally, increasing the width of D-mode device (driver No. 2) can reduce the rise time to less than 0.5 μs compared to the driver No.1.

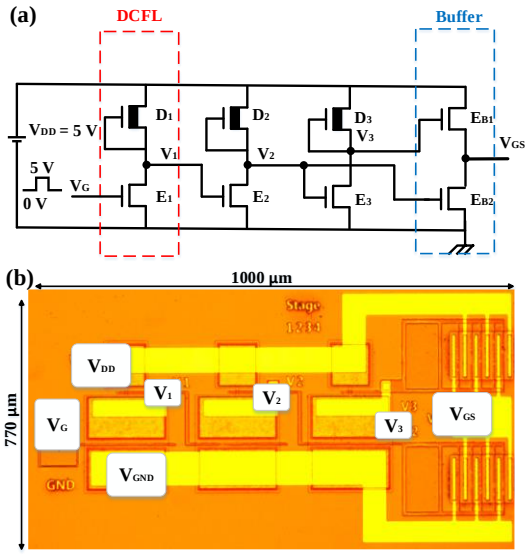

Fig. 3. The circuit diagram and a photograph of driver No. 3.

With a buffer stage (width=500 μm), the rise time of driver No. 3 can be greatly reduced from 2 μs (V_1, V_2 and V_3) to less than 0.5 μs (V_4) in Fig. 4 (c). A large buffer width of driver No. 4 (width=2000 μm) can further decrease rise time owing to large gate charging current. However, a very large gate voltage overshoot and an obviously increased oscillation during turn-on transition are observed in Fig. 4 (a) (red line). Unfortunately, the gate voltage overshoot can seriously damage or breakdown switching transistor,[25] especially for low gate voltage tolerance transistors, such as HEMTs or P-GaN HEMTs, which usually show $V_{G,\,max}$ less than 7 V.[26] GaN-based MIS-HEMTs can increase the gate overshoot tolerance due to the insertion of gate dielectric, which can increase gate swing.[27] Additionally, the increased oscillation of driver No. 4 during turn-off transition can cause false turn-on of switching transistor, which can consequently affect the duty cycle and stability of converters. Hence, the balance between switching speed and oscillation requires careful consideration during the design process of the driver.

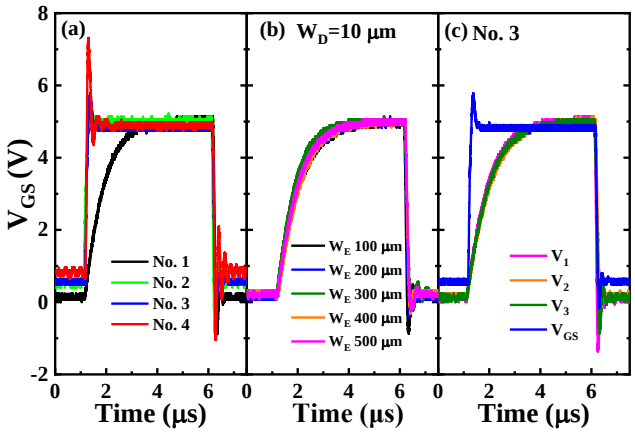

Fig. 4 (a) Dynamic V_{GS} waveforms of 4 drivers. (b) Output waveforms with different E-mode width of discrete single-stage inverters fabricated on the same chip (width of D-mode: W_D=10 μm). (c) Voltage waveforms at each stage of driver No. 3, where $V_{G,max}$=5 V, V_{DD}=5 V, f = 100 kHz, and duty cycle=0.5 at room temperature.

The relationship between the size of gate drivers and rise/fall time in Fig. 4 can be qualitatively analyzed by the following discussion. The τ_{rise} and τ_{fall} estimation is derived based on a nMOSFET inverter consisting of an enhancement-mode nMOS driver and a depletion-mode nMOS load,[28] the detailed derivation is shown in the appendix. The time calculation of GaN drivers with DCFL inverters w/o buffer stage (No. 1 and No. 2) can be expressed by following formulas:

$$\tau_{rise} = \frac{C_L}{\mu_D C_{ob}} \left(\frac{L}{W}\right)_D f\left(V_{DD}, V_{T,D}\right) \tag{1}$$

$$f\left(V_{DD}, V_{T,D}\right) = \frac{1}{\left|V_{T,D}\right|}\left[\ln\left(\frac{7.2V_{DD}}{2\left|V_{T,D}\right| - 0.9V_{DD}} + 9\right)\right]$$

$$\tau_{fall} = \frac{C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_E g(V_{DD}, V_{T,E}) \tag{2}$$

$$g\left(V_{DD}, V_{T,E}\right) = \frac{1}{(V_{DD} - V_{T,E})}\left\{\frac{2\left(V_{T,E} - 0.1V_{DD}\right)}{(V_{DD} - V_{T,E})} + \ln\left(\frac{2(V_{DD} - V_{T,E}) - 0.1V_{DD}}{0.1V_{DD}}\right)\right\}.$$

The rise and fall time of drivers with a buffer stage (No. 3 and No. 4) can be obtained by formula (3) and (4), respectively:

$$\tau_{rise} = \frac{2C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_{EB1} F\left(V_{DD}, V_{T,E}\right) \tag{3}$$

$$F\left(V_{DD}, V_{T.E}\right) = \frac{V_{DD} - 2V_{T,E}}{\left|0.1V_{DD} - V_{T,E}\right|\left(0.9V_{DD} - V_{T,E}\right)}$$

$$\tau_{fall} = \frac{C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_{EB2} g(V_{DD}, V_{T,E}) \tag{4}$$

$$g(V_{DD}, V_{T,E}) = \frac{1}{(V_{DD} - V_{T,E})} \left\{ \frac{2\left(V_{T,E} - 0.1V_{DD}\right)}{(V_{DD} - V_{T,E})} + \ln\left(\frac{2(V_{DD} - V_{T,E}) - 0.1V_{DD}}{0.1V_{DD}} \right) \right\}.$$

C_L is the output load capacitance, C_{ox} is the oxide capacitance, C_{br} is the barrier capacitance leading to modification of oxide capacitance as $C_{ob} = (C_{ox}^{-1} + C_{br}^{-1})^{-1}$, C_{int} is the interconnection capacitance, μ_D and μ_E are the channel mobility of D-mode and E-mode devices, respectively. $V_{T,D}$ and $V_{T,E}$ are the threshold voltages of D-mode and E-mode devices, respectively. $\left(\frac{L}{W}\right)_D$ is the gate length/width ratio of D-mode devices, and $\left(\frac{L}{W}\right)_E$ is the gate length/width ratio of E-mode devices. $f(V_{DD,}V_{T,D})$, $g(V_{DD,}V_{T,E})$ and $F(V_{DD,}V_{T,E})$ are size-independent functions. Considering that the C_L is increasing with the device dimensions, formula (1) and (2) without (w/o) buffer can be simplified as (5) and (6), while formula (3) and (4) with buffer can be simplified as (7) and (6), respectively:

$$\tau_{rise} \propto \frac{C_{int}}{\mu_D C_{ob}} \left(\frac{L}{W}\right)_D f(V_{DD}, V_{T,D}) \tag{5}$$

$$\tau_{fall} \propto \frac{L^2}{\mu_E} g(V_{DD}, V_{T,E}) \tag{6}$$

$$\tau_{rise} \propto \frac{2L^2}{\mu_E} F\left(V_{DD}, V_{T,E}\right). \tag{7}$$

For drivers w/o buffer stage (No. 1 and No. 2), τ_{rise} is only related to the size of the D-mode active resistor. Considering all drivers share the same gate length, τ_{rise} is thus inversely proportional to the gate width of D-mode devices from formula (5). This can

explain that driver No. 2 with a larger D-mode width has a smaller rise time compared to driver No. 1 in Fig. 4 (a). In formula (6), τ_{fall} is only related to the E-mode transistors due to discharging current during falling edge. τ_{fall} is proportional to L^2 and independent on gate width, which coincides with Fig. 4 (a), where all drivers have the similar fall time of less than 0.5 μs regardless of width difference.

For gate drivers with buffer stage (No. 3 and No. 4) in formula (7) and (6), both rise time and fall time are independent on gate width. Additionally, the rise time of driver No. 3 can be obviously reduced due to high charging current through upper E_{B1} device during rising edge, compared to driver No. 1.

Fig. 5 shows dynamic V_{GS} waveforms at high temperatures from 25 °C, and 100 to 250 °C in 50 °C steps. In Fig. 5 (a), driver No. 1 shows obvious temperature degradation, especially for the rise time. In Fig. 5 (b), the rise time of driver No. 2 has been improved compared to No. 1, but still shows temperature degradation of rise time to some extent. In Fig. 5 (c), with a buffer stage, driver No. 3 shows negligible rise time degradation even at high temperatures. This indicates the importance of the buffer stage, especially for high temperature application, because the gate overshoot will be reduced due to current degradation at high temperatures leading to a low switching-on speed of the driver in Fig. 5 (b). However, if the buffer width is too large, such as for driver No. 4 in Fig. 5 (d), the gate overshoot and oscillation will be of concern as previously discussed, despite of the high switching speed. The low on-state $V_{GS,max}$ around 3 V of dirver No. 4 at 250 °C is possibly caused by the large width (2000 μm) of E-mode devices in DCFL inverters, which might lead to a higher V_{OL} of the inverters, and V_{OL} is the voltage when output is low. As shown in Fig. 5, driver No. 1 and No. 3 (E-mode width 200 μm in DCFL inverters) have a V_{OL} of less than 0.25 V, while driver No. 2 and driver No. 4 (E-mode width 2000 μm in DCFL inverters) have a V_{OL} of 0.5~0.8 V. The higher V_{OL} of DCFL inverters in driver No. 4 might cause the E_{B2} device flow nonegligible current at on-state, especially at high temperatures due to the negative shift of the threshold voltage.[17] This might consequently cause the lower $V_{GS,max}$ at 250 °C of driver No. 4 at on-state due to voltage division principle.

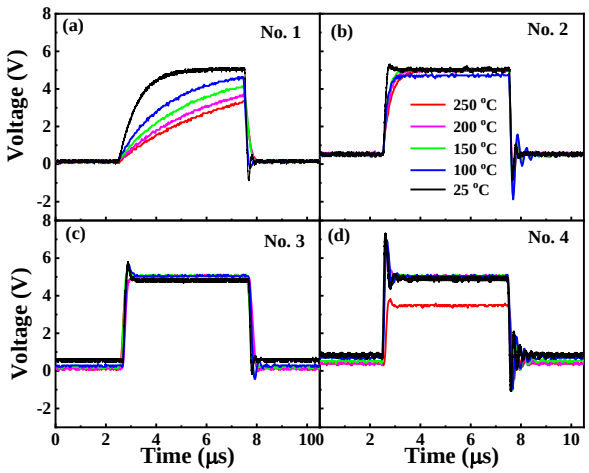

Fig. 5. Dynamic V_{GS} waveforms of different gate drivers at temperature range from 25 °C to 250 °C. (a) Driver No. 1, (b) driver No. 2, (c) driver No. 3 and (d) driver No. 4.

Fig. 6 shows calculated rise times and fall times of four drivers at various temperatures, where the calculation refers to the first slope of rising edge (10 % to 90 % stable V_{OUT}) and falling edge (90 % to 10 % stable V_{OUT}), regardless of oscillation. At room temperature, all drivers show similar fall times around 0.1 μs, hence we use fall time here for simplicity to estimate the load capacitance C_L using either formula (2) or (4). Given V_{DD}=5 V and $V_{T,E}$=1.5 V, the g(V_{DD}, $V_{T,E}$) is calculated to be 0.89 V^{-1}. Furthermore, μ_E=251 $cm^2V^{-1}s^{-1}$ as reported using a similar digital-etching technique.[21] C_{ox} was measured as 308 $nFcm^{-2}$ from a recessed Al_2O_3/GaN MOS capacitor, which was fabricated on the same chip with GaN ICs. Using the parameter values above, the calculated C_L is found to be around 6 nF (Fig. 6). Driver No. 1 shows the highest rise and fall times, and driver No. 4 with a large buffer width shows the lowest fall and rise times of less than 0.2 μs due to high current transition. Driver No. 2 shows small fall times but relatively high rise times of more than 0.5 μs at 250 °C, due to the absence of the buffer stage as in previous discussion. Driver No. 3 shows relatively low rise and fall times of less than 0.25 μs across the whole temperature range.

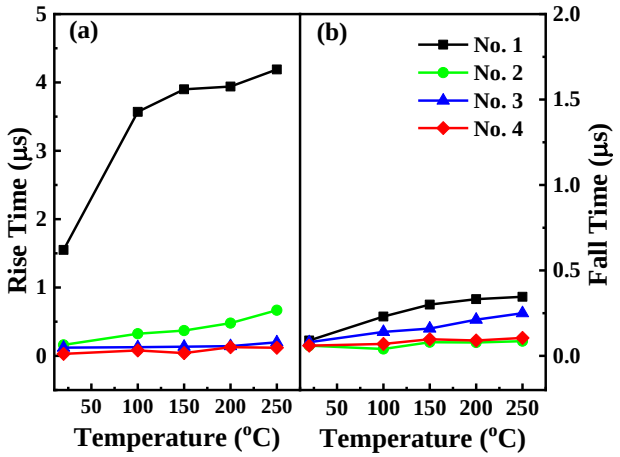

Fig. 6. Rise/fall time of different drivers at various temperatures. (a) Rise time (10 % to 90 % stable V_{OUT}), (b) fall time (90 % to 10 % stable V_{OUT}). The load capacitance C_L is ~6 nF as calculated.

3.2 Boost Converters with Integrated Drivers

Fig. 7 (a) shows the circuit diagram of the boost converter with an E-mode switching transistor S_0 (width = 5 mm) and an integrated driver No. 3. The gate drivers and the power transistor S_0 were fabricated on the same chip, but here we separate them in the diagram in order to distinguish the two parts. Fig. 7 (b) shows the experimental set up for the boost converter. The inductor *L*, diode *D*, capacitor *C* and the load resistor *R* were integrated on a PCB board, the gate drivers and transistor S_0 were externally connected with external components of the PCB board using probes, and the negative electrodes of power supply are connected to the common ground GND. Differential voltage probes were used to detect the dynamic inductance and output voltages in an oscilloscope.

Fig. 8 shows the output converter and inductance waveforms of driver No. 3 with duty cycles of 0.1, 0.3, 0.5 and 0.7 at V_{GS}, these corresponding to duty cycles of 0.9, 0.7, 0.5 and 0.3 at V_G, respectively. For direct comparison between four drivers with different numbers of inverter stages, here we use duty cycles of output waveform V_{GS} of each driver. In Fig. 8, the output voltage V_{OUT} is increasing with duty cycles as expected. At room temperature, converter results of different drivers are shown in Fig. 9. The calculated values using formula (8) at different duty cycles are also plotted in the same figure for comparison. The total area

under the inductor voltage waveform is zero whenever the converter operates in steady state, so the following formulas can be obtained:

$$\int_0^{T_S} v_L(t)\,dt = 0$$

$$V_{IN} \times \mathrm{D} + \left(V_{IN} - V_{OUT} - 0.7\right) \times \left(1 - D\right) = 0$$

$$V_{OUT} = \frac{V_{IN}}{1-D} - 0.7 . \tag{8}$$

In Fig. 9, the experimental results are comparable with calculated values at low duty cycles (D= 0.1 and 0.3), but lower than calculated values at high duty cycles (D= 0.5 and 0.7). The discrepancies increase with duty cycles, which might be caused by reduced inductance voltage at on-state as shown in the inset of Fig. 9 (referring to enlarged view of Fig. 8). The reduced inductance voltage might be caused by increased on-state voltage drop between drain and source of the S_0 transistor, owing to not low enough on-state resistance in this work. However, this does not affect the studies of gate drivers because all drivers share the same switching transistor S_0 in this work.

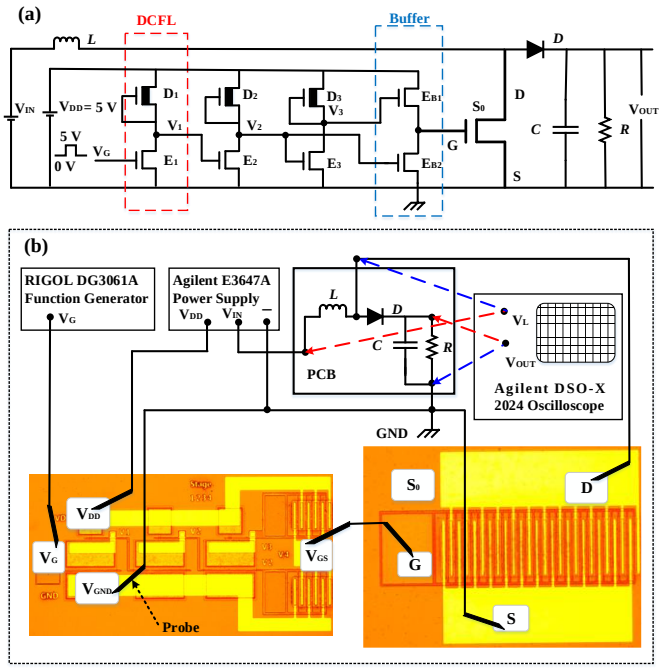

Fig. 7. (a) The circuit diagram of the DC-DC boost converter with the integrated driver No. 3. (b) The experimental set up of converter test. (The parameters of discrete components are: L=1 mH, C =10 µF, R=500 Ω. V_{IN}=V_{DD}=5 V, f =100 kHz, the threshold voltage V_F of the

discrete diode D (FR107) is +0.7 V, the maximum DC voltage and current are 1000 V and 1 A, respectively).

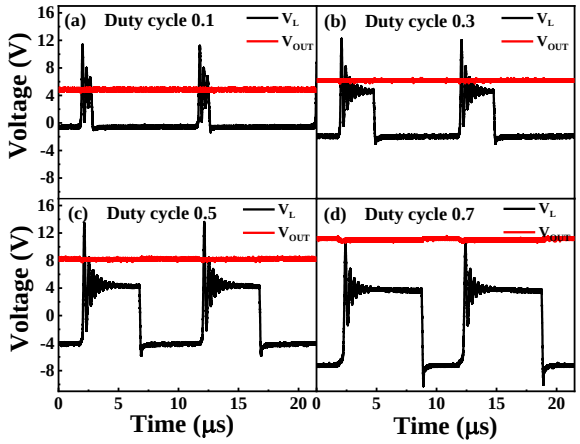

Fig. 8. Waveforms of boost converters with integrated gate driver No. 3 at different duty cycles. (a) D= 0.1, (b) D= 0.3, (c) D= 0.5 and (d) D= 0.7. V_L is the voltage at the inductor *L*.

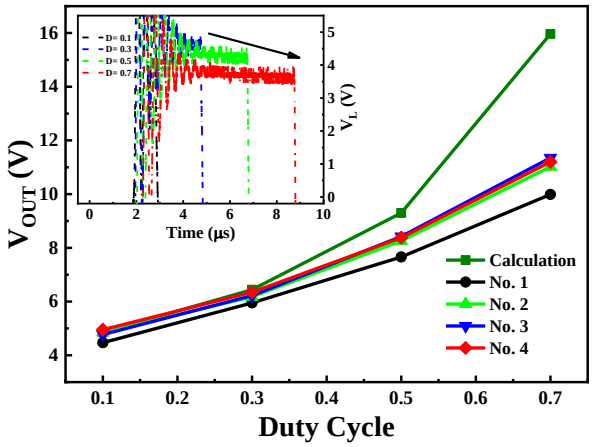

Fig. 9. Experimental and theoretical results of V_{OUT} vs duty cycle from different drivers at room temperature. The inset shows an enlarged view of V_L at different duty cycles from Fig. 8.

The high temperature tests of converters were performed on a high temperature probing stage over a wide temperature range from 25 °C, and 100 to 250 °C in 50 °C steps. Only the GaN chip with integrated gate drivers and power transistor was heated on the hot stage; the PCB board was off the probing stage and was externally connected to GaN power ICs using probes. The converter results at various temperatures are shown in Fig. 10. All drivers show

slight degradation at high temperatures even at 250 °C, indicating obvious advantages of GaN-based drivers for HT converters in applications under extreme environment, such as oil drilling, aviation and hybrid electric vehicles. Among four different drivers, driver No. 1 shows obvious temperature degradation at 100 °C. Driver No. 4 (large buffer width) shows temperature dispersion at high duty cycle (D= 0.7) due to current degradation caused by the large gate overshoot and oscillation. Driver No. 3 (small buffer width) shows the smallest temperature dispersion, which might be attributed to high switching speed and small gate voltage overshoot/oscillation as previously discussed.

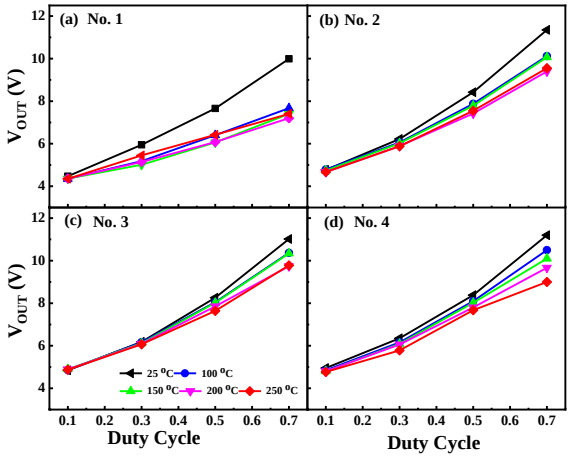

Fig. 10. Temperature dependent boost results with different gate drivers. (a) Driver No. 1, (b) driver No. 2, (c) driver No. 3 and (d) driver No. 4.

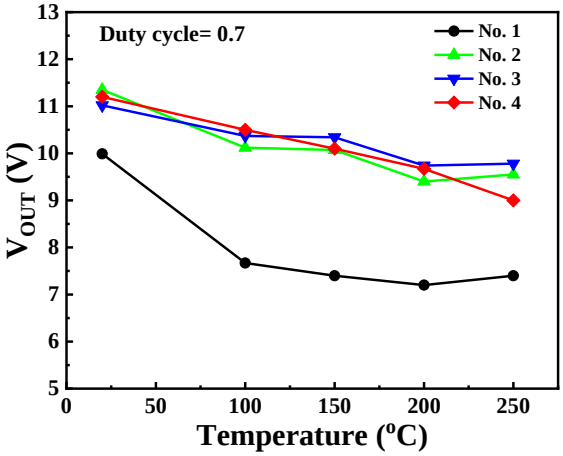

Fig. 11. Temperature dependent boost results for different drivers at duty cycle D= 0.7.

Fig. 11 shows temperature dependent boost results for different drivers with a duty cycle of 0.7. It is apparent that driver No. 1 has the lowest output voltages through the whole temperature range due to the large rise times shown in Fig. 6 (a). All other drivers show slight reduction of V_{OUT} with increasing temperature, likely to be due to temperature degradation of rise/fall times or due to current degradation for both D-mode and E-mode devices (shown in Fig. 2) caused by degradation of channel mobility of transistors. Another factor is the negative threshold voltage shift at high temperatures, which can increase the output voltage.[17] The latter can explain the slight increase of output voltages at 250 °C in Fig. 11. Overall, driver No. 3 shows the comparably highest output voltages among the four drivers, especially at high temperatures above 150 °C. At 25 °C, driver No. 3 has an output voltage of 11 V, and only 11% of output voltage reduction has been observed at 250 °C, indicating good thermal stability for HT gate driver applications.

4. Conclusions

The GaN-based high-temperature gate driver presented in this paper is a preliminary research effort to design gate driver for HT GaN-based DC-DC converters. A 100 kHz, 5 V/11 V (V_{IN}/V_{OUT}) boost converter with the optimized integrated-driver has been proposed in this paper. The driver can maintain high output voltages over a wide temperature range of up to 250 °C. Only 11% reduction of output voltage at 250 °C has been observed compared to room temperature value, indicating a novel application of HT gate driver for GaN-based converters under extreme environment conditions.

Acknowledgments

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Appendix

The rise and fall time are derived based on an nMOSFET inverter consisting of an enhancement-mode nMOS driver and a depletion-mode nMOS load. As a first order of magnitude approximation, the drain current formula of a silicon nMOSFET is employed. The current-voltage equations to be used for the depletion-mode load transistor are identical to those of the enhancement-mode device, with the exception of the sign of threshold voltages.[28] At room temperature, the current-voltage equations of an enhancement nMOSFET can be expressed as:

$$I_D(\text{lin}) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left[2(V_{GS}-V_T)V_{DS}-V_{DS}^2\right] \qquad V_{GS}>V_T,\ V_{DS}<V_{GS}-V_T$$

$$I_D(\text{sat}) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_T)^2 \qquad V_{GS}>V_T,\ V_{DS}>V_{GS}-V_T$$

C_{ox} of D-mode Al_2O_3/AlGaN/GaN MIS-HEMTs should be replaced by C_{ob} due to the contribution of AlGaN barrier to gate capacitance.[29] C_{ox} is the oxide capacitance, C_{br} is the barrier capacitance and $C_{ob} = (C_{ox}^{-1} + C_{br}^{-1})^{-1}$. The gate capacitance of the E-mode Al_2O_3/GaN MIS-HFETs is only determined by C_{ox} due to the absence of the barrier layer.

Four different drivers can be classified into two types, DCFL inverters without (w/o) buffer and DCFL inverters with buffer. Assume that all D-mode and E-mode devices have the same threshold voltages $V_{T,D}$ and $V_{T,E}$, respectively. The diagrams of DCFL inverters w/o buffer are shown in Fig. I.

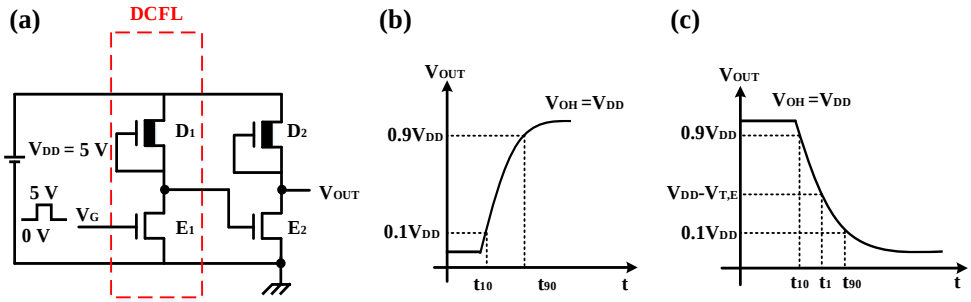

Fig. I (a) The circuit diagram of a gate driver with DCFL inverters w/o buffer (No. 2). The diagrams of rise time (b) and fall time (c).

Fig. I (b) shows the diagram of the rise time. E_2 device operates in off-state and flows negligible current, V_{DD} is charging output through D_2. For D_2 device, $V_{OUT}=V_{DD}-V_{DS}$, $V_{GS}=0$

V, $V_{DS} < V_{GS} - V_T = 0 - (-8) = 8V$. So D_2 device always operates in linear region during the rise time (0.1 V_{OH} to 0.9 V_{OH}).

$$\mathrm{dt} = -\frac{C_L}{i_{ds}(t)} dV_{out}$$

$$\int_{t_{10}}^{t_{90}} dt = -\int_{0.1V_{DD}}^{0.9V_{DD}} \frac{2C_L}{\mu_D C_{ob}} \left(\frac{L}{W}\right)_D \frac{dV_{out}}{\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right]}$$

$$\tau_{rise} = \frac{C_L}{\mu_D C_{ob}} \left(\frac{L}{W}\right)_D \frac{1}{(V_{GS} - V_{T,D})} \left[\ln\left(\frac{7.2V_{DD}}{2(V_{GS} - V_{T,D}) - 0.9V_{DD}} + 9\right)\right]$$

So the rise time of DCFL inverters w/o buffer can be expressed by:

$$\tau_{rise} = t_{10-90} = \frac{C_L}{\mu_D C_{ob}} \left(\frac{L}{W}\right)_D f(V_{DD}, V_{T,D}) \tag{1}$$

$$f(V_{DD}, V_{T,D}) = \frac{1}{|V_{T,D}|} \left[\ln\left(\frac{7.2V_{DD}}{2|V_{T,D}| - 0.9V_{DD}} + 9\right)\right].$$

Fig. I (c) shows the diagram of fall time. D_2 device operates in linear region; note that here we do not consider small current of D_2 device during fall time. The output is discharging through E_2. For E_2 device, $V_{OUT}=V_{DS}$, $V_{GS} \approx V_{DD}$. When $V_{OUT}<V_{DD}-V_{T,E}$, E_2 device operates in linear region, while when $V_{OUT} > V_{DD}-V_T$, E_2 device operates in saturation region. Fall time (0.9 V_{OH} to 0.1 V_{OH}) can be obtained by following formulas:

$$\mathrm{dt} = -\frac{C_L}{i_{ds}(t)} dV_{out}$$

$$t_{90-1} = \int_{t_{90}}^{t_1} dt = -\int_{0.9V_{DD}}^{V_{DD}-V_{T,E}} \frac{2C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_E \frac{dV_{out}}{(V_{GS} - V_{T,E})^2}$$

$$t_{90-1} = \frac{2C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_E \frac{(V_{T,E} - 0.1V_{DD})}{(V_{DD} - V_{T,E})^2}$$

and,

$$t_{1-10} = \int_{t_1}^{t_{10}} dt = -\frac{2C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_E \int_{V_{DD}-V_{T,E}}^{0.1V_{DD}} \frac{dV_{out}}{\left[2(V_{GS} - V_{T,D})V_{DS} - V_{DS}^2\right]}$$

$$t_{1-10} = \frac{C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_E \frac{1}{(V_{DD} - V_{T,E})} \left[\ln\left(\frac{2(V_{DD} - V_{T,E}) - 0.1V_{DD}}{0.1V_{DD}} \right) \right].$$

So the total fall time of DCFL inverters w/o buffer can be expressed as:

$$\tau_{fall} = \frac{C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_E \frac{1}{(V_{DD} - V_{T,E})} \left\{ \frac{2\left(V_{T,E} - 0.1V_{DD}\right)}{(V_{DD} - V_{T,E})} + \ln\left(\frac{2(V_{DD} - V_{T,E}) - 0.1V_{DD}}{0.1V_{DD}} \right) \right\}$$

$$\tau_{fall} = \frac{C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_E g(V_{DD}, V_{T,E}) \tag{2}$$

$$g(V_{DD}, V_{T,E}) = \frac{1}{(V_{DD} - V_{T,E})} \left\{ \frac{2\left(V_{T,E} - 0.1V_{DD}\right)}{(V_{DD} - V_{T,E})} + \ln\left(\frac{2(V_{DD} - V_{T,E}) - 0.1V_{DD}}{0.1V_{DD}} \right) \right\}.$$

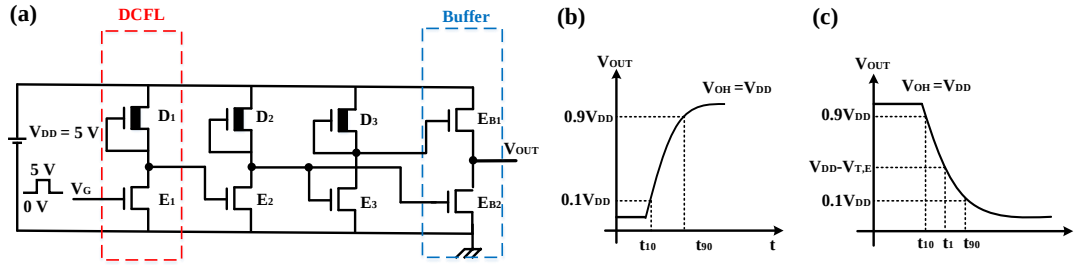

Fig. II (a). The circuit diagram of a gate driver with DCFL inverters with buffer (No. 3). The diagrams of (b) rise time and (c) fall time.

Fig. II (a) shows the circuit diagram of a gate driver with DCFL inverters with buffer stage. Fig. II (b) shows the diagram of rise time. Assuming that E_{B2} flows negligible current and operates in pinch-off region, V_{DD} is charging output through E_{B1}. For E_{B1}, V_T>0 V, $V_G \approx V_{DD}$, V_{GS}-V_T=V_{DD}-V_{OUT}-V_T. So V_{DS}=V_{DD}-V_{OUT}>V_{GS}-V_T, so E_{B1} operates in saturation region during rise time (0.1 V_{OH} to 0.9 V_{OH}). Hence,

$$\mathrm{dt} = -\frac{C_L}{i_{ds}(t)} dV_{out}$$

$$t_{10-90} = \int_{t_{10}}^{t_{90}} dt = -\int_{0.1V_{DD}}^{0.9V_{DD}} \frac{2C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_{EB1} \frac{dV_{out}}{\left(V_{GS} - V_{T,E}\right)^2}$$

$$t_{10-90} = \frac{2C_L}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_{EB1} \frac{V_{DD} - 2V_{T,E}}{\left|0.1V_{DD} - V_{T,E}\right| \left(0.9V_{DD} - V_{T,E}\right)}.$$

So the rise time of DCFL inverters with buffer stage can be expressed as:

$$\tau_{rise} = \frac{2C_L}{\mu_E C_{ox}} \left(\frac{L}{W} \right)_{EB1} F\left(V_{DD}, V_{T,E}\right) \tag{3}$$

$$F\left(V_{DD}, V_{T,E}\right) = \frac{V_{DD} - 2V_{T,E}}{\left|0.1V_{DD} - V_{T,E}\right|\left(0.9V_{DD} - V_{T,E}\right)}.$$

Fig. II (c) shows the diagram of fall time. Following the similar discussion as in Fig. I, the output is discharging through E_{B2} and the fall time of DCFL inverters with buffer stage can be expressed by:

$$\tau_{fall} = \frac{C_L}{\mu_E C_{ox}} \left(\frac{L}{W} \right)_{EB2} g(V_{DD}, V_{T,E}) \tag{4}$$

$$g(V_{DD}, V_{T,E}) = \frac{1}{(V_{DD} - V_{T,E})} \left\{ \frac{2\left(V_{T,E} - 0.1V_{DD}\right)}{(V_{DD} - V_{T,E})} + \ln\left(\frac{2(V_{DD} - V_{T,E}) - 0.1V_{DD}}{0.1V_{DD}} \right) \right\}.$$

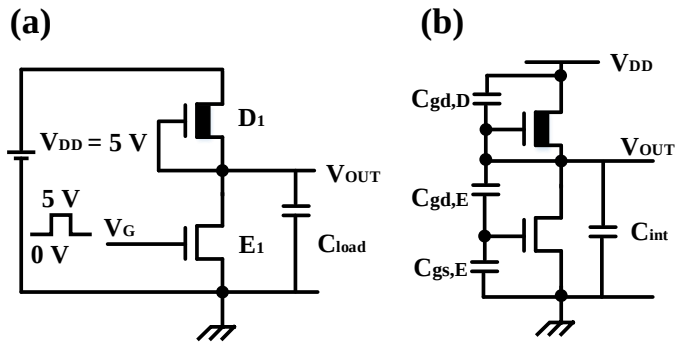

Fig. III (a) Circuit diagram of a DCFL inverter, and including (b) parasitic device capacitances. $C_{gd,D}$ is the gate-to-drain capacitance of D-mode devices, $C_{gd,E}$ is the gate-to-drain capacitance of E-mode devices, $C_{gs,E}$ is the gate-to-source capacitance of E-mode devices, and C_{int} is the interconnect capacitance.

Fig. III shows the capacitance of a single DCFL inverter, C_L or C_{load} consists of intrinsic and extrinsic capacitances. C_{int} is the interconnect capacitance. Note that since GaN transistors do not have gate overlap capacitances unlike Si-MOSFETs, we only consider oxide capacitances over the gate area:

$$C_L = C_{gd,D} + C_{gd,E} + C_{gs,E} + C_{int}$$

$$C_L = C_{ob} W_D L_D + C_{ox} W_E L_E + C_{int}$$

We assume that $C_{int} \leq C_g$, so the load capacitance is mainly dominated by gate

capacitances and normally $C_{gs} > C_{gd}$, so gate source capacitance C_{gs} dominates gate capacitance.[30)]

During rise time, the E-mode transistor is in off-state, V_{DD} is charging C_L through the D-mode device, so the impact of $C_{ox}W_EL_E$ on the τ_{rise} can be ignored, $C_{gs} \approx 0$ F due to gate-source connection, so C_L is dominated by C_{int} during rise time, and formula (1) can be simplified as:

$$\tau_{rise} \propto \frac{C_{int}}{\mu_D C_{ob}} \left(\frac{L}{W}\right)_D f(V_{DD}, V_{T,D}) . \tag{5}$$

During fall time, C_L is discharging mainly from the E-mode device, so $C_{gs,E}$ dominates the gate capacitance. Thus formula (2) for fall time can be simplified as:

$$\tau_{fall} \propto \frac{C_{ox} W_E L_E}{\mu_E C_{ox}} \left(\frac{L}{W}\right)_E g(V_{DD}, V_{T,E})$$

$$\tau_{fall} \propto \frac{L^2}{\mu_E} g(V_{DD}, V_{T,E}) . \tag{6}$$

Similarly, we take a first order of magnitude approximation for DCFL inverters with buffer stage, considering the width of buffer stage to be larger than the width of inverters. So formulas (3) and (4) can be simplified as (7) and (6), respectively:

$$\tau_{rise} \propto \frac{2L^2}{\mu_E} F\left(V_{DD}, V_{T,E}\right) . \tag{7}$$

Here, $f(V_{DD,}V_{T,D})$, $g(V_{DD,}V_{T,E})$ and $F(V_{DD,}V_{T,E})$ are size-independent functions.

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